3-MS/s Hybrid Imager with 3-Frame On-chip Storage for Ultra High-speed Radiography

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The design, fabrication and performance of a 3MHz, 720×720-pixel hybrid visible imager will be discussed. The imager consists of a 0.25μm CMOS readout integrated circuit (ROIC) indium bump-bonded to a pixellated silicon photo-sensor. This camera system is primarily intended to record images formed on a fast scintillator obtained in flash proton radiography (pRAD) experiments. The repetition rate in pRAD can be as high as 2.8 MHz (358 ns) with 40 ns wide beam bursts which leads to minimum pulse integration time of 180ns. To address the resulting high instantaneous read-out rate of 1-Tbit/s the imager was designed with three-frame in-pixel analog storage.

The 26 μm pitch pixel camera is operated in a burst/snapshot mode and features in-pixel correlated double sampling (CDS) for each of the three acquired frames. The CDS operation is necessary to overcome the kTC noise of the integrating node to achieve high dynamic range. A 65- or 30-fps continuous readout mode is also provided. The back-illuminated silicon array has close to 100% fill factor, while anti-reflective coating maximizes its quantum efficiency at 80%-to-95% over the scintillator emission wavelength range. The ROIC is a 720×726, two-side buttable 19×19mm^2 chip, it incorporates on-chip 12-bit analog-to-digital converter. Timing and circuit biasing are also generated on-chip, and special attention has been given to the power distribution of the pixel-array and snapshot signal buffers. This “photons-to-bits” system-on-chip approach has resulted in a compact and low power camera.

The camera performed well in the initial tests, showed no radiation related latch-ups or excessive starring. And it has been included into the regular pRAD experimental set-up. Further extensions of the imager to the full resolution of 1440×1440 pixels (tiling or CMOS stitching) and the options for increasing the number of stored frames (through 3-D interconnect) will also be described.