IWORID

July 5th 2005, ESRF, GRENOBLE

FLIP CHIP INTEGRATION: STATUS AND FUTUR TRENDS

OUTLINE

- INTRODUCTION
  - What is packaging, the different levels
  - Evolution of packaging
  - The Flip chip technology
- DIFFERENT FLIP CHIP METHODS
  - Associated technologies
  - Advantages and Limitations
- INNOVATIVE TECHNOLOGIES

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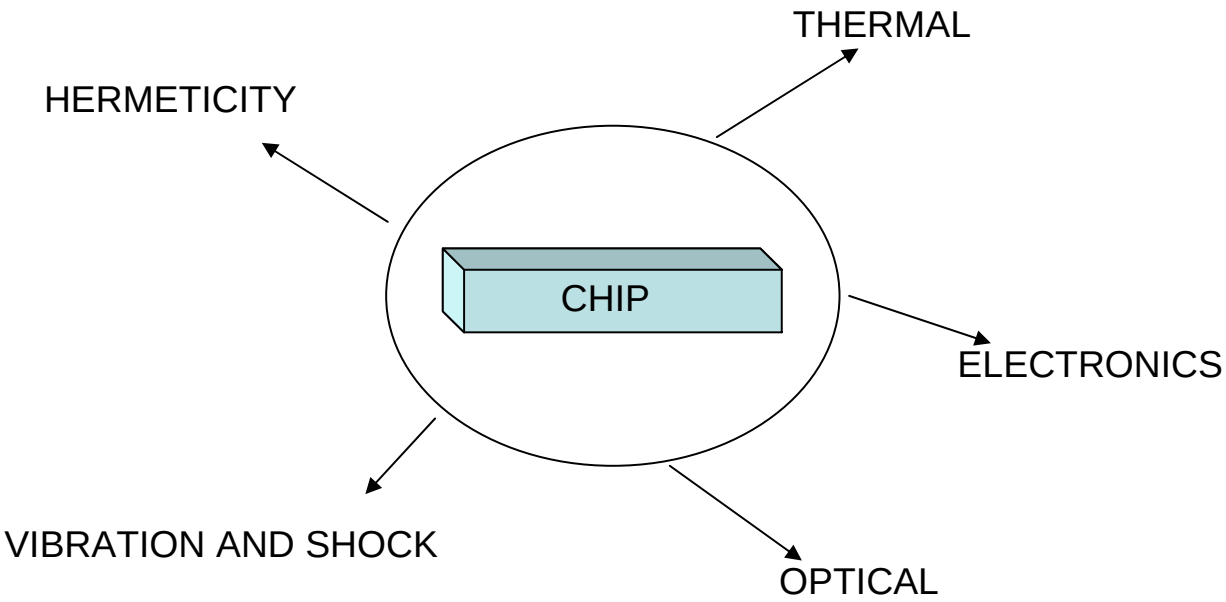
What is Packaging



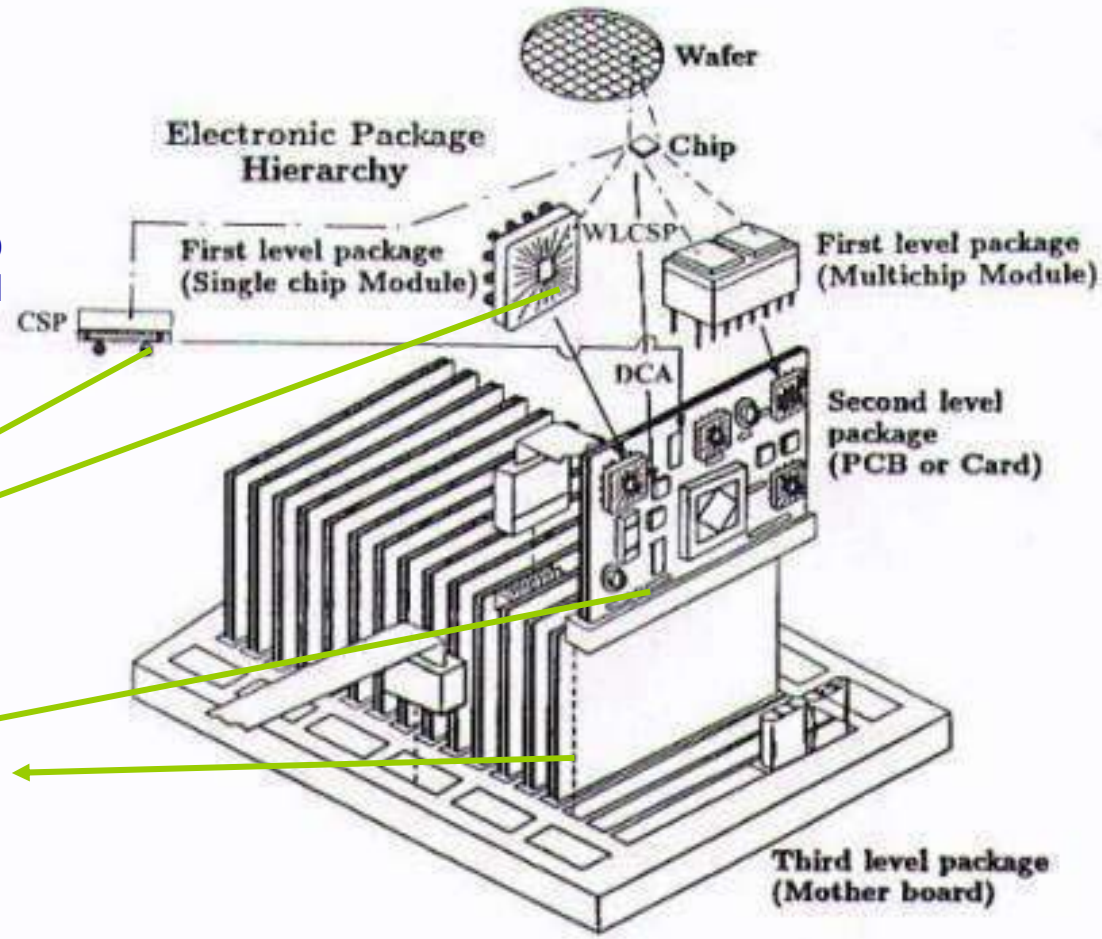
Different packaging levels

Level 0 : Silicon Chip
- Integrated Circuit etched on a Silicon Wafer

Level 1 ; « Chip Carrier »
- Ceramic or Plastic Encapsulent with electrical connections

Level 2 : Connection over the PCB

Level 3 : Functional system
- interconnection of several sub systems to achieve a functional system



Flip chip
CSP BGA

Connectors

Source: TUMALA

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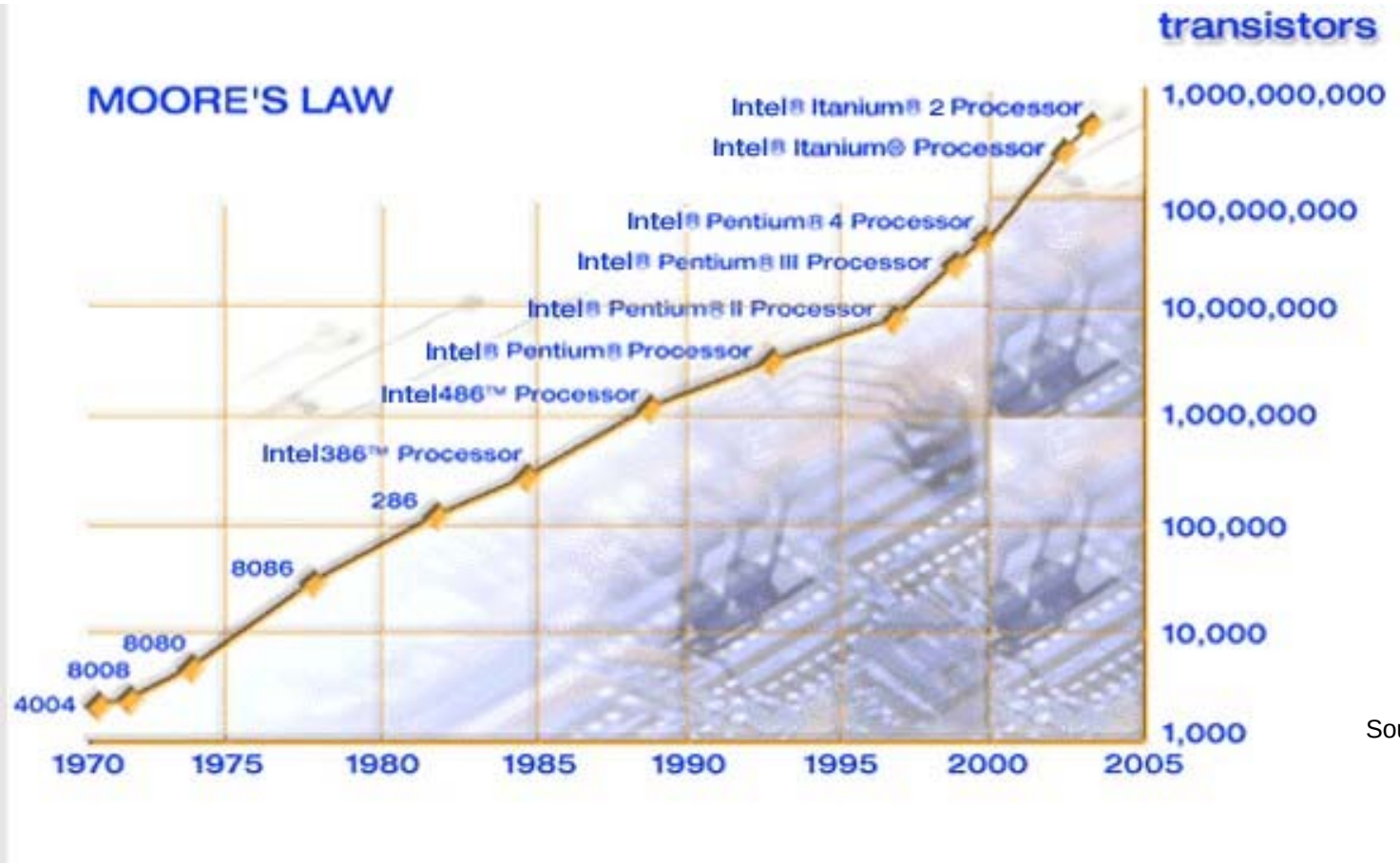
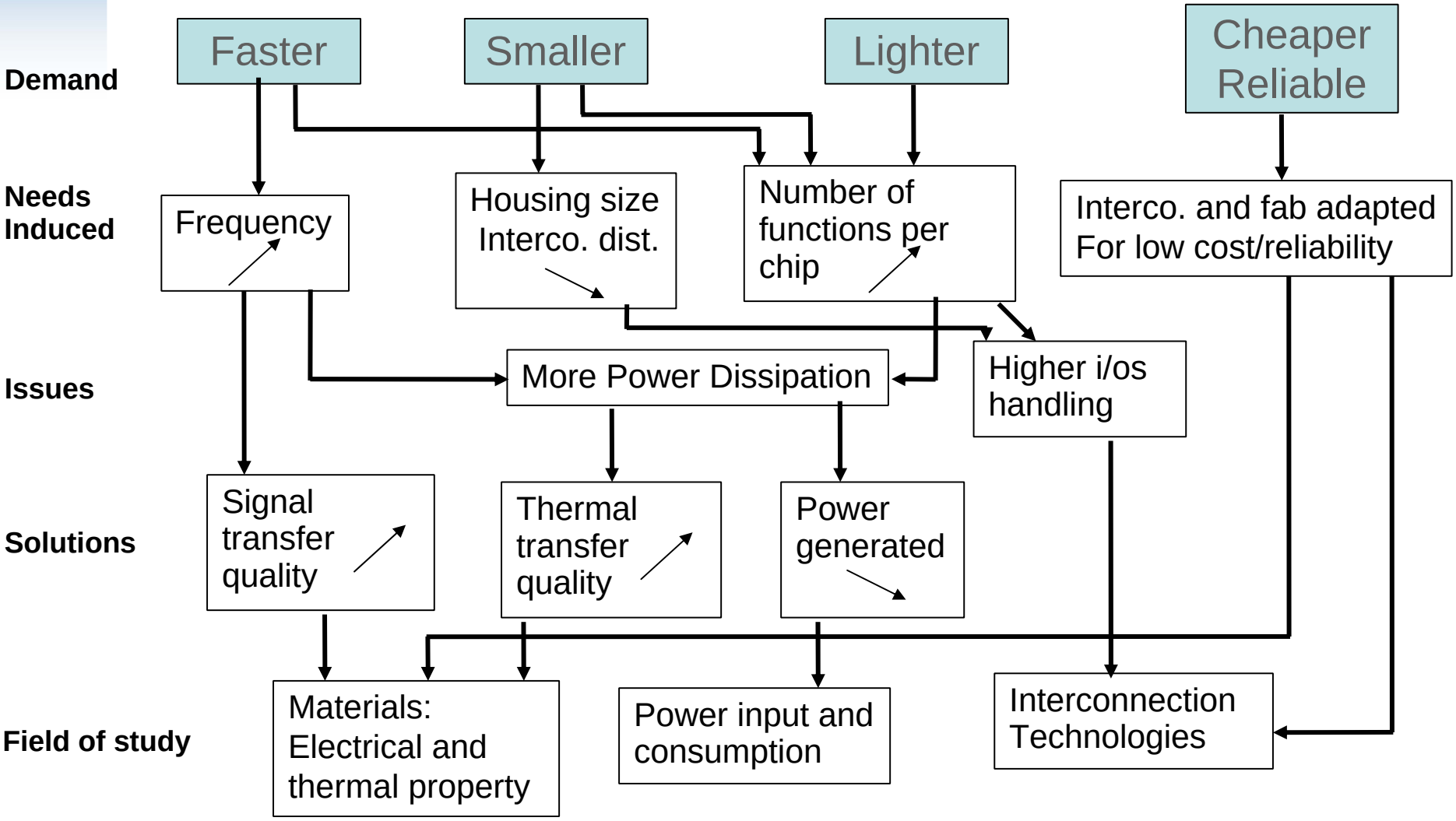
Increased Chip Density



Source Intel

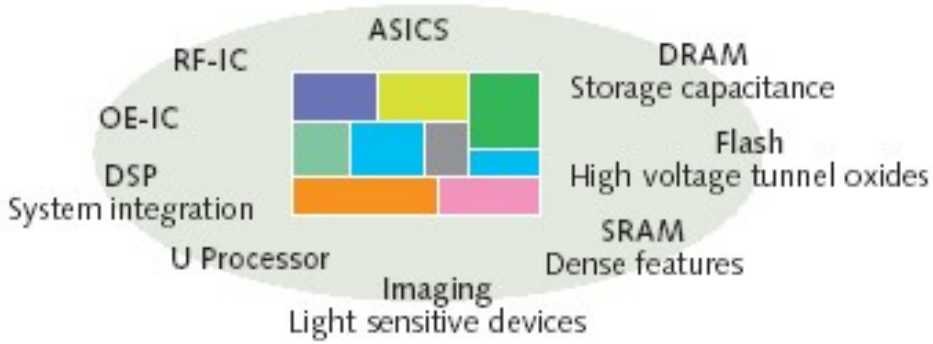
Packaging: New Requirements



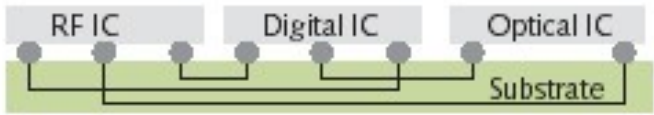
Source: M. Massena

SOP, SiP, MCM, SOC : lots of solutions

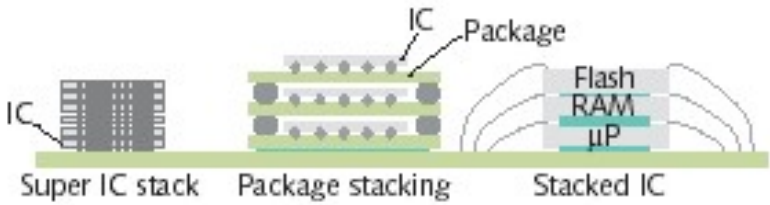
SOC
Complete system on one chip



MCM
Interconnected components



SIP
Stacked chip/package



SOP
- Optimizes functions between ICs andpackage
- Miniaturizes systems

Best of Both IC & Package

Source Georgia Tech

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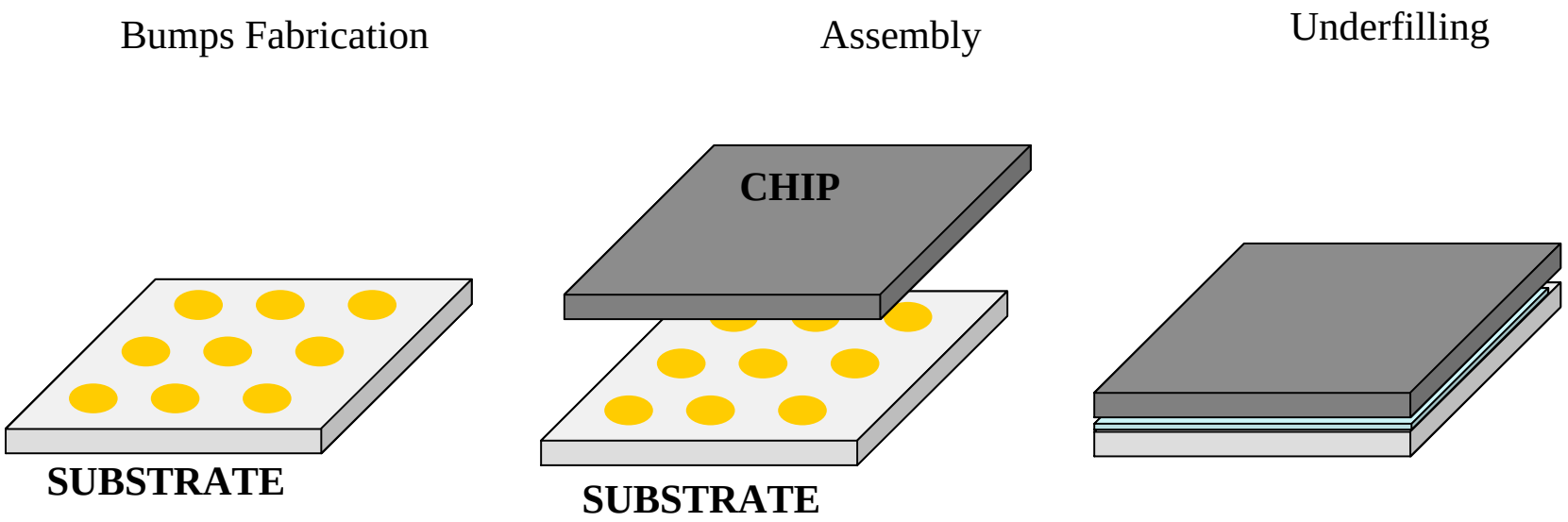
What is Flip Chip

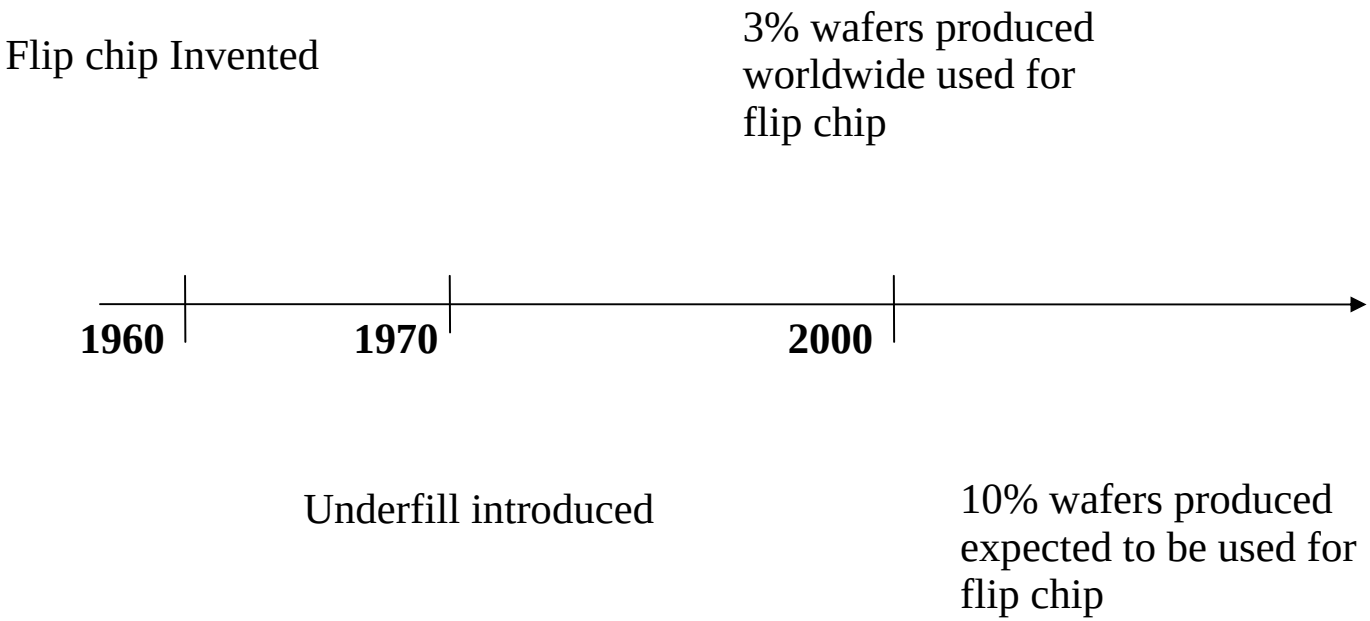
- **Face down** Electrical connection
- Chip over a substrate
- **Array** type connection (Not peripheral) using **bumps**
- Usually with an **underfill** (Reliability)



A little bit of History

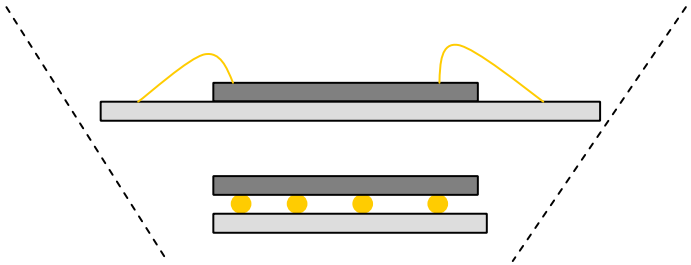
- Flip chip: invented by IBM in early 60's

  Controlled Collapse Chip Connection (C4- 1964)

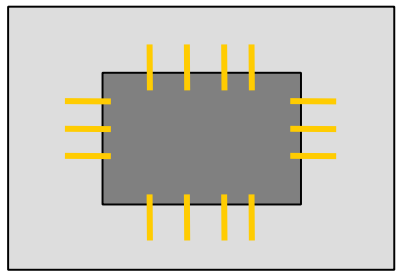


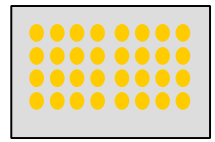
Flip Chip vs Wire Bonding

SIZE REDUCTION



NUMBER OF I/O's





Smaller pitch

- **Flip Chip**
  - Size reduced
  - Higher integration
  - Shorter connection length
  - Smaller pitch
  - Self alignment
  - collective process
  - Efficient heat dissipation

- **Wire Bonding**
  - Industrially proven
  - Moderate cost
  - Reliability
  - Compatibility (housings, connectors)
  - Standard metallurgy (no post process)

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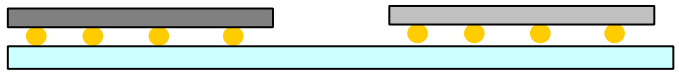
Flip Chip : The different techniques

- Solder bump Flip Chip
- Stud bump Flip Chip
- Polymer bump Flip Chip
- Anisotropic Conductive film Flip Chip

Chip over circuit

Chip and circuit over a substrate



Solder Bump Flip Chip: The different steps

- ASIC and chip Post Process
- Solder bump deposition
- Solder Reflow
- Flip Chip assembly
- Underfilling

Solder Bump Flip Chip: The Post Process

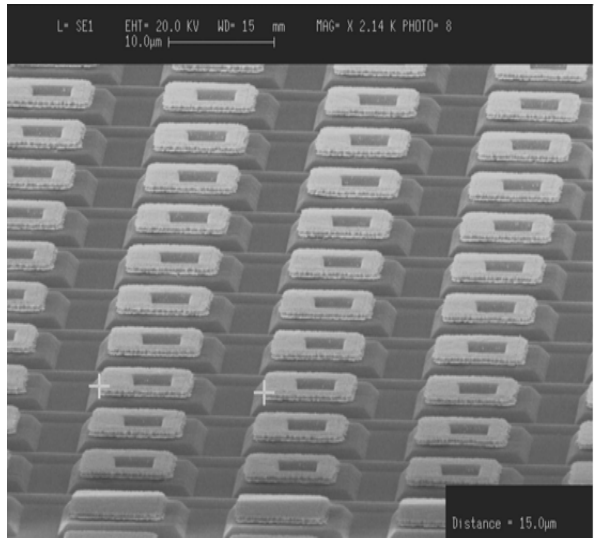
Sputtering Deposition

3 Metal layers deposited

Lithographie

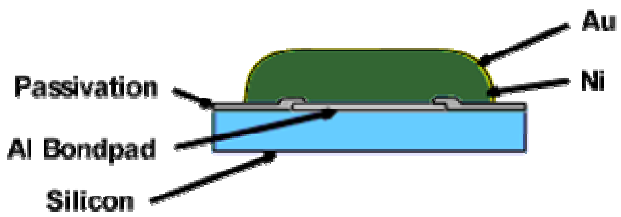
Metal Etching

15 µm pitch Ti/Pd/Au UBM

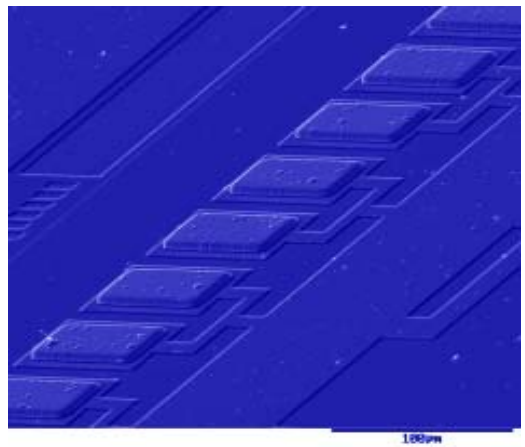


Source: LETI

Electroless deposition (NiAu)



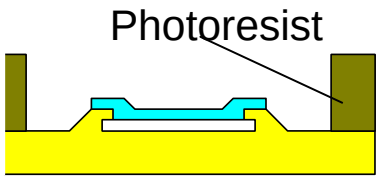
1µm to 30µm Ni
0,05µm Au



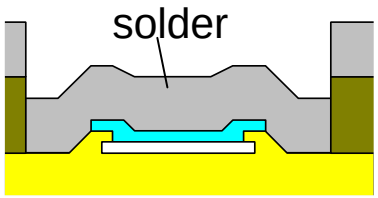
Source: Pac Tech

Solder deposition and Solder Reflow

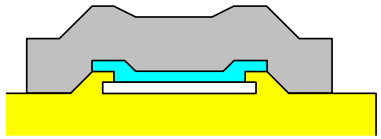
Evaporation Method



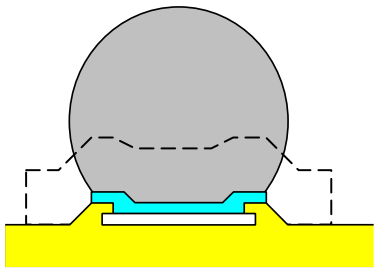
Al pad with UBM



solder deposition

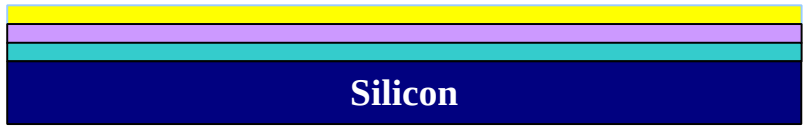


Photoresist Lift-off

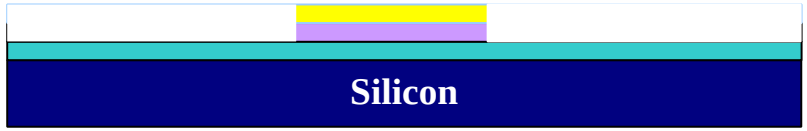


solder reflow

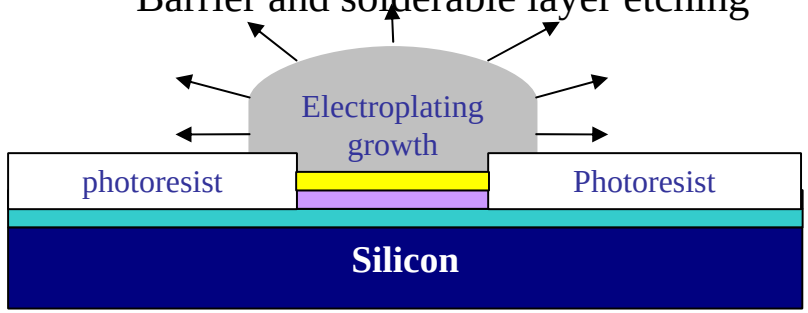
Electroplating Method



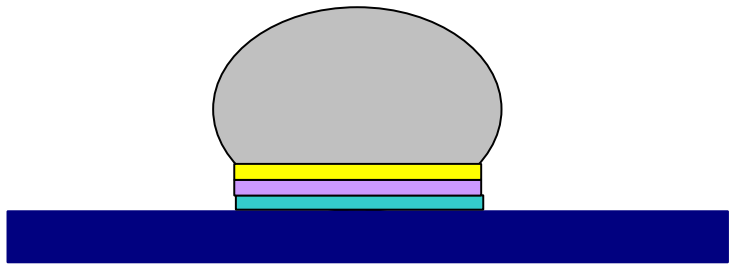
UBM deposition



Barrier and solderable layer etching



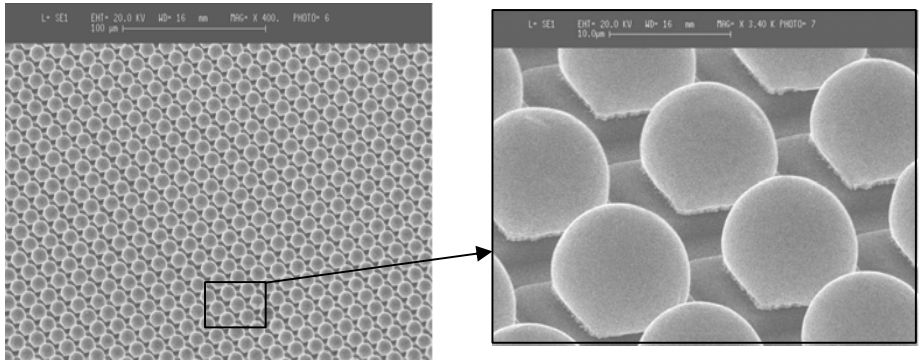
Photoresist deposition, electroplating growth



Solder reflow and adhesion layer etching

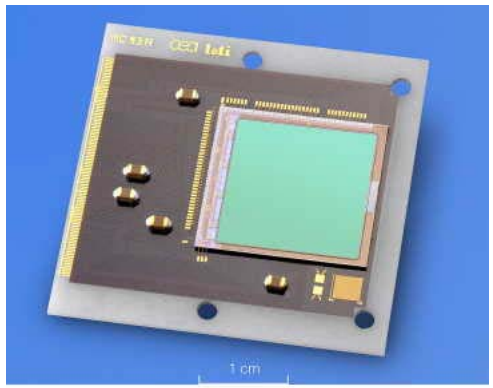
Solder deposition and Solder Reflow

Example of indium vapor deposition at leti



Indium Micro-bumps
(SEM Photography)

Méga Pixel IRFPA 1024 x 1024 : pitch =15 µm



Spectral band: 3 - 5 µm -
Cutoff frequency: 5.5 µm

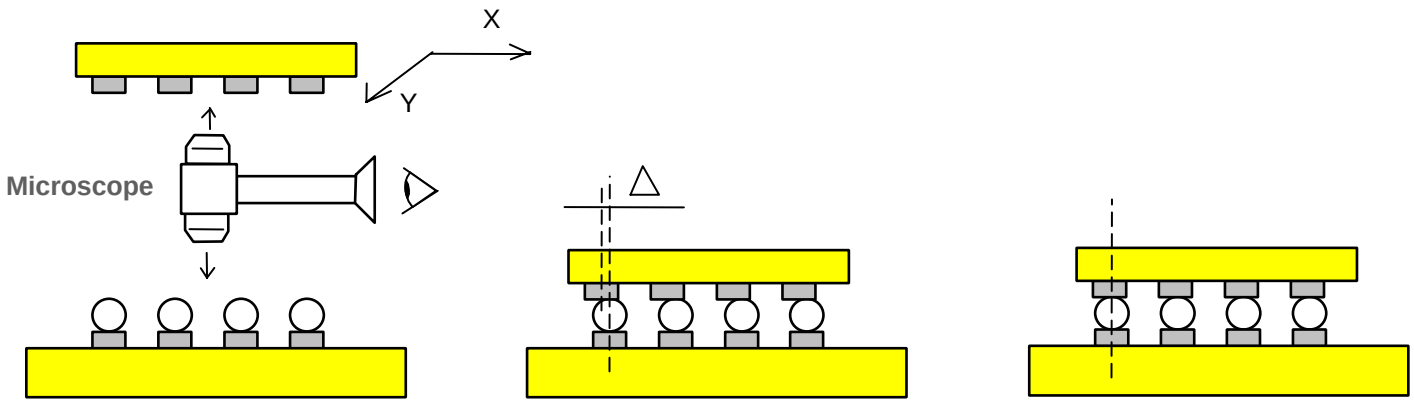
Night view
Operability 99.8%
NETD 20mK

Solder deposition method comparison

	Advantages	Disadvantages	Size
• **Evaporation**	- thin film process uniformity, flexibility	- cost, time	10 µ-100 µ
• **Electroplating**	- low cost,fine pitch	- flexibility	10-200 µ
• **Screen Printing**	- cost, simplicity production	- pitch limitation	150-1000 µ
• **Jet printing**	- limited number of Bumps, no mask	- pitch limitation	> 150 µ

Solder Flip Chip Assembly

A three step process



1st Step:
Alignment

2nd Step:
Positioning

3rd Step:
Reflow solder and self-alignment

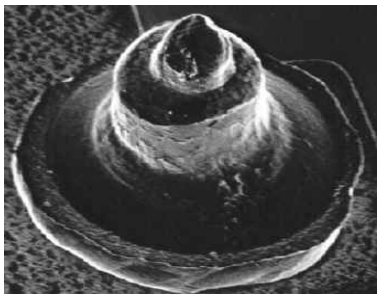
Solder Flip Chip: Associated Issues

- Temperature process: CTE mismatch
- Flux activated process: cleaning issues
- Large chip size: constraint, shear stress, reliability issues
- Yield: underfilling step necessary

Flip Chip using Stud Bump

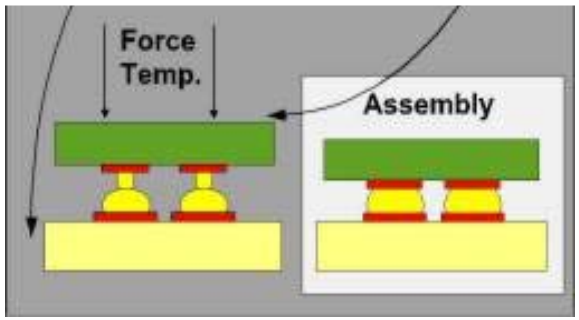
- Conductive gold bumps on the die
- Directly on the Al pad
- Thermomechanical or Adhesive attachment

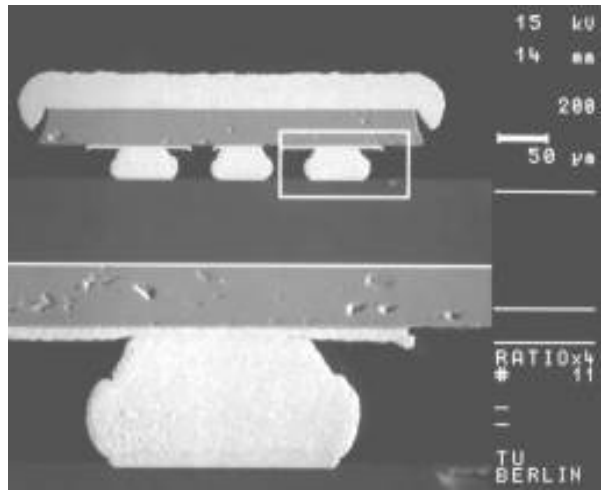
Gold Stud Bump



Source: www.flipchips.com

Thermocompression assembly





Source: IZM

Stud Bump Flip Chip:

Advantages

- No wafer post process
- Bumping equipment widely available
- No fluxing

Limitations

- Serial process (low to medium volume production, 24 bumps/sec.)
- No self-alignement
- Minimum Pitch 50-60 µm
- High Temperature & Force applied

Polymer Flip Chip

Principle

- Conductive particles filled adhesive
- Particles: Typically Silver

Dispense

- Dispensing
- Screen Printing

Assembly

- Curing

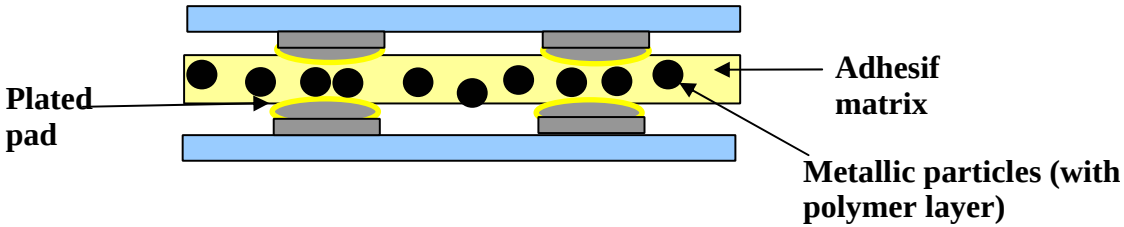
Advantages

- Low temperature process
- Low cost

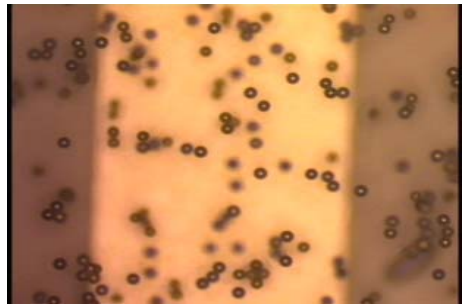
Flip Chip with Anisotropic Conductive Film

different types:

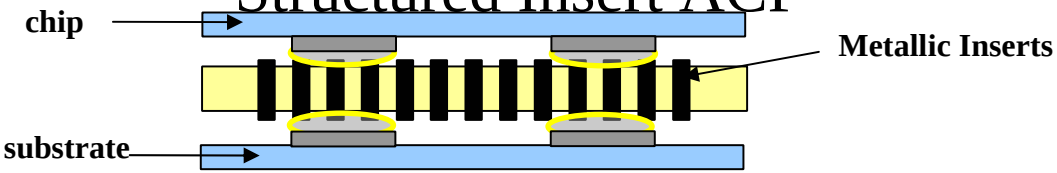
Trapped particles ACF



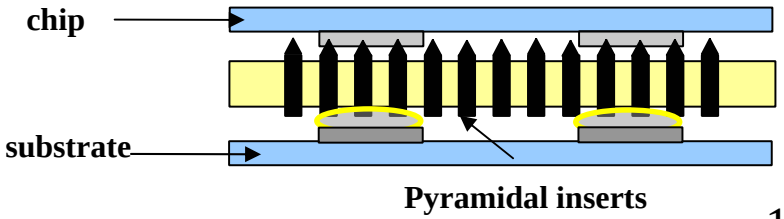
5552 R Film

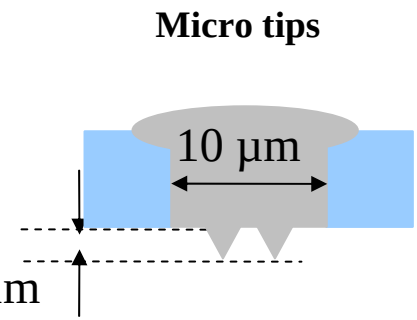


Structured Insert ACF

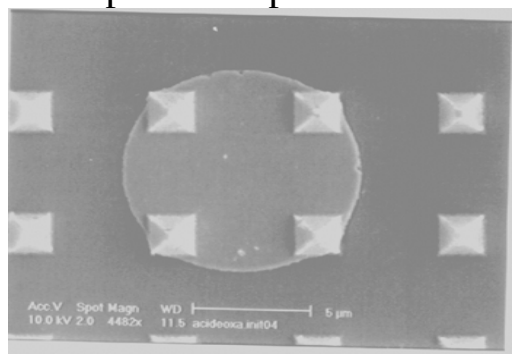


Micro tips insert ACF





Micro tips developed at LETI



ACF Flip Chip

Advantages

- No underfilling step
- Low temperature process (100°C)
- No post process with micro tips inserts

Limitations

- Fine pitch
- Post process
- No self alignment
- Pressure applied
- Electrical contact

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Issues and Limitations

- CTE Mismatch
  - Size limitation
  - Reliability issues
- Small Pitch
  - Alignment
  - Cleaning
- Yield
  - No inspection possible
- Circuit tiling
  - Need solution for 3D Interconnection
- Cost

Comparison of the Different Methods

	DISPENSE AND PROCESS	***PITCH***	***CONTACT RESISTANCE***	***ASSEMBLY AND TEMPERATURE***	***RELIABILITY***	***COST***
SOLDER FLIP CHIP	Screen printing, Electroplating, vapor deposition, jet dispensing. Post process required	150µm 15 µm and over	1.2 mΩ	Depends on solder Reliable low temperature solder: In 180˚C process Self alignment Cleaning required	Reliable with underfilling Repairable	Depends on solder Expensive with In
STUD BUMP FLIP CHIP	Standard wire bonding equipment No post process	60 µm		Over 200˚C Pressure applied (75to100g/bumps) No self alignment No cleaning	Reliable Not repairable	40$/wafer with 250000 bumps/wafer source: flipchips.com
POLYMER FLIP CHIP	Screen printing, dispensing Post process required	125 µm	5-10 mΩ	<100˚C No self alignment No cleaning	Limited reliability for dense connection Not repairable	Low cost
ACF	Commercially available films Post process required	50µm	50 mΩ (with 10 particles/pads)	100˚C Pressure applied (15-30 kg/cm^2) No self alignment No cleaning required	Limited reliability for dense connection Not repairable	Low cost

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New Flip Chip approach: Nano-connections

- Carbon Nanotubes (Georgia Tech)

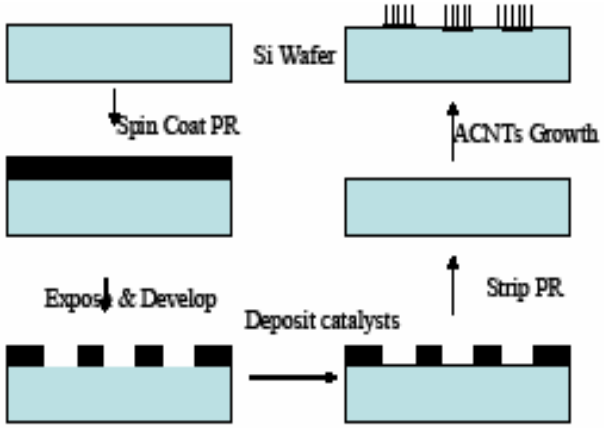
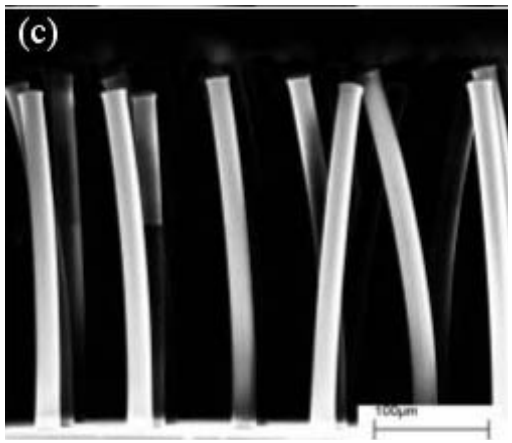
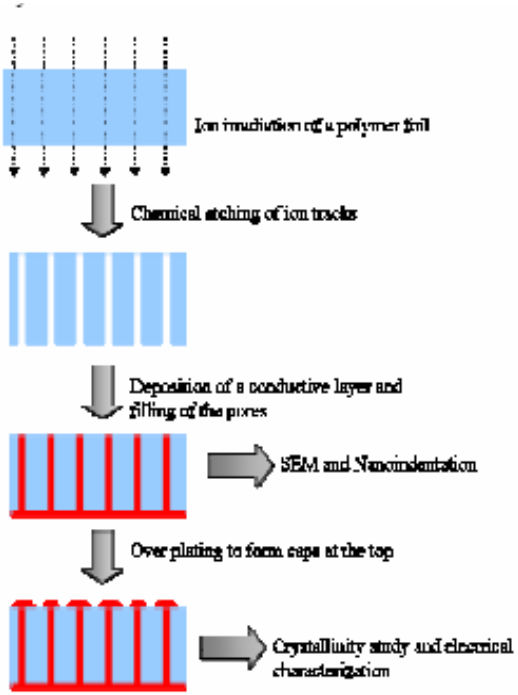


Fig. 6. Scheme of the CNT pillar growth



- Copper Nanotubes (Georgia Tech)



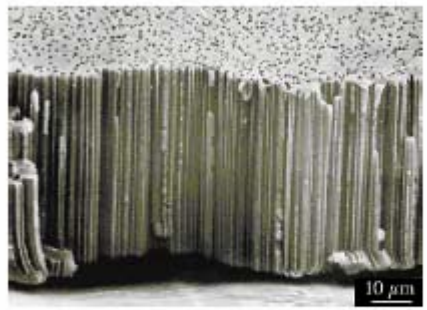
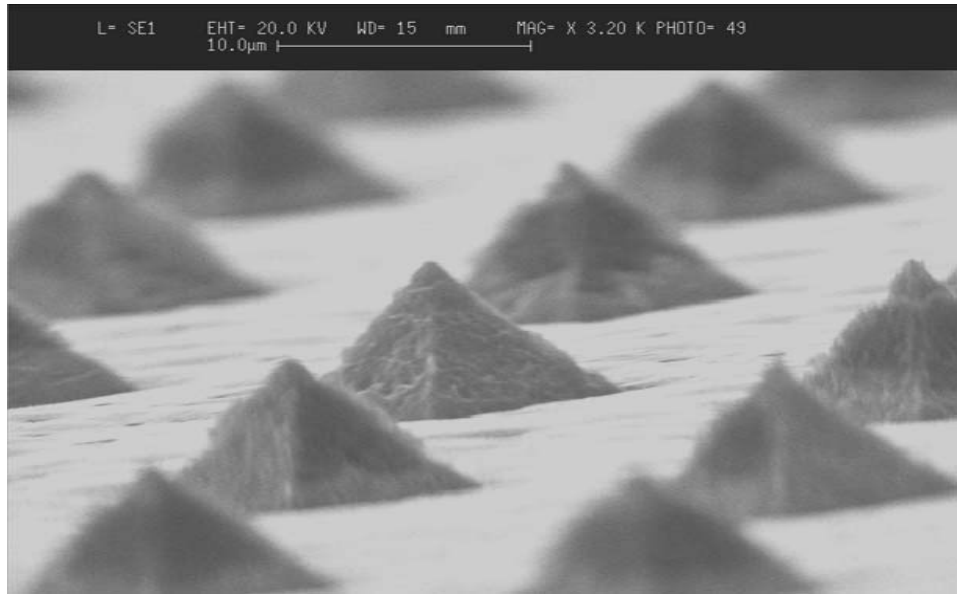


Figure 2: SEM image of side view of the etched polymeric membrane

New Flip Chip approach: Nano-connections

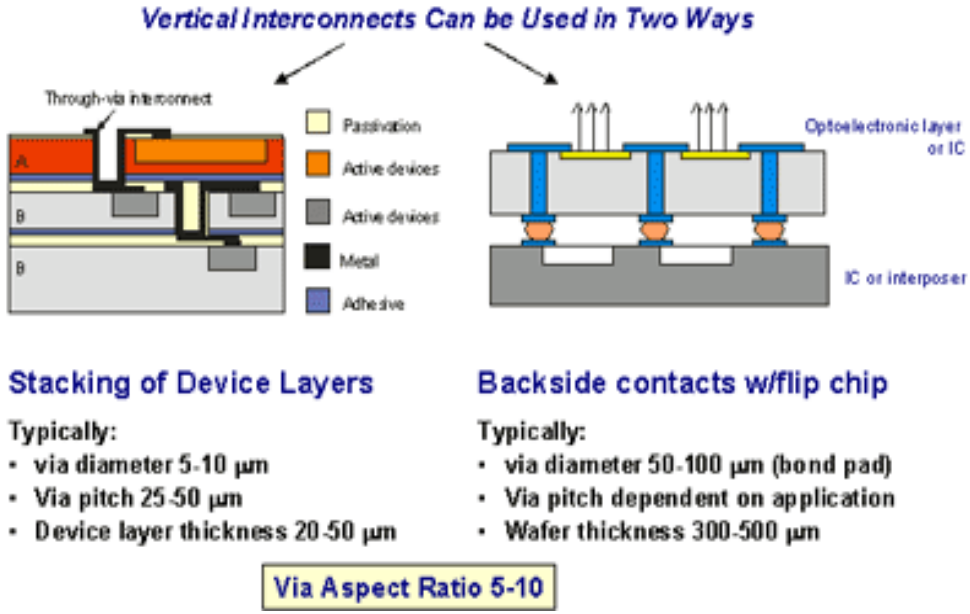
- Solder Micro Tips (LETI)
  - Fabrication demonstrated
  - Assembly tested
  - Fluxless assembly
  - No underfill



3D-Interconnections

- Based on through vias filled with metal (Cu)
- Strong technical challenges (vias, vertical wall metalization and passivation)
- Cell phone application (Japan)

- Exemple: MCNC Research Center:



Conclusion: Future Integration Trends

- **Total Integration with SOC**
  - Very complexe
  - Mix backend and frontend technologies

- **Development of Wafer Level Packaging and SIP**
  - More and more heterogeanous functions on the same substrate (MEMES, MOEMS, IC's)
  - Denser packaging: 3D connections

- **New connection technique for Flip Chip assembly**

Thanks for your attention

QUESTIONS ?